REMARKS

Claims 1-11 and 13-36 are pending in the present application.

In the office action mailed March 26, 2004 (the "Office Action"), claims 1-36 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,697,063 to Zhu (the "Zhu patent).

Claims 1, 10, and 18 are not anticipated by the Zhu patent because the Zhu patent fails to disclose the combinations of limitations recited by the respective claims. The Zhu patent is directed to a graphics rendering pipeline that utilizes screen space tiling (SST) to improve memory bandwidth utilization for frame buffer accesses and further utilizes a double-z rendering scheme to decouple scan conversion/depth buffer processing from the rasterization/shading process. The Examiner has cited to various material in the Zhu patent as disclosing the limitations recited in claim 1, 10, and 18. However, the cited material has been mischaracterized by the Examiner, and as a result, the cited material does not disclose the limitations as purported by the Examiner.

For example, the Examiner cites to col. 6, lines 2-50 as teaching "shifting a transformed primitive by a first sub-pixel offset rendering the shifted primitive to generate values for pixels of a first intermediate image shifting the transformed primitive by a second sub-pixel offset." *See* the Office Action at page 2. Reviewing the material cited by the Examiner reveals that an overview of SST is provided. As explained in the Zhu patent, "[s]creen space tiling (SST) partitions a screen into disjoint (rectangular) regions (called tiles). It bins all geometries in screen space into tiles that the geometries intersect. Primitives crossing multiples tiles will be binned in all relevant tiles." *See* col. 6, lines 3-7. Figure 3 is referenced in describing an example of SST, and the rest of the cited material describes the "binning process" used in the rendering pipeline. This material fails to disclose shifting a transformed primitive to first and second offsets. It further fails to disclose shifting the transformed primitive by a sub-pixel offset.

The Examiner also cites to col. 34, line 50-col. 36, line 3 as disclosing "rendering the shifted primitive to generate values for pixels of a second intermediate image." *See* the Office Action at page 2. This material, however, fails to describe rendering a geometric primitive that has been shifted by an offset in order to generate pixels for a second intermediate image. The material cited by the Examiner is directed to Figures 14-16, which illustrate various

embodiments of anti-aliased multipass rendering. A first anti-aliasing scheme directly composites the color contribution of individual passes of fragments into the color buffer. In contrast, a second anti-aliasing scheme merges color contribution from all passes for each fragment into one color, and then composites that color value with the value in the corresponding color buffer location. Both of these anti-aliasing schemes are illustrated in Figure 14. Figure 15 illustrates a modification of the second anti-aliasing scheme that combines the first and second schemes. An upper limit is put in place on the number of fragments that are stored in the multipass buffer such that whenever the number of fragments exceeds the buffer size of the multipass buffer, multi-pass merging is deactivated. Compositing of the fragments then takes place in the color buffer. As a result, the second anti-aliasing scheme is utilized until the number of fragments fills the multipass buffer, at which the first anti-aliasing scheme is then utilized. Figure 16 illustrates one more modification where an arithmetic unit is shared between the multi-pass buffer and the color buffer. None of this material cited by the Examiner discloses generating pixels for a second intermediate image by rendering a shifted geometric primitive. The material merely describes various anti-aliasing schemes that can be implemented in the rendering pipeline.

The Examiner further cites to col. 5, lines 45-67 as disclosing "combining the values for the respective pixels of the first and second intermediate images to determine the values for the pixels of the image." *See* the Office Action at page 2. The cited material, however, discloses the combining of visibility information with the tile geometries for each tile of the SST so that only visible geometries are set up for rasterization. That is, only visible fragments are fully rasterized and shaded. The visible fragments of each tile are sent to a blending engine for alpha blending of the incoming fragments. This material does not address combining the values for the respective pixels of first and second intermediate images, where the intermediate images result from rendering a geometric primitive at first and second offsets. Rather, the material cited by the Examiner merely discloses alpha blending of the visible fragments of each tile in order to resolve and output pixel colors into a frame buffer.

After reviewing the material cited by the Examiner, none of the limitations for which the material has been cited are disclosed. Moreover, the cited material further fails to disclose issuing geometric primitives of a scene a plurality of times or reissuing geometric

primitives for each sampling location of a sampling pattern, which are recited by claims 10 and 18, respectively. The Examiner has failed to show that the Zhu patent describes every limitation of the combination, and in the particular arrangement recited by the respective claims. For the foregoing reasons, claims 1, 10, and 18 are patentably distinct from the Zhu patent. Therefore, the rejection of claims 1, 10, and 18 under 35 U.S.C. 102(e) must be withdrawn.

Claims 24 and 33 are similarly patentably distinct from the Zhu patent. Claim 24 recites a graphics system comprising a primitive set-up engine for reading the geometric data and generating transformed geometric data therefrom for a new coordinate space, a rendering stage coupled to the primitive set-up engine to issue the geometric primitives in the new coordinate space a plurality of times, the rendering stage further configured to shift the geometric primitive a sub-pixel offset, and calculate values for pixels representing the shifted geometric primitive, and a buffer coupled to the rendering stage into which the values for the pixels calculated by the rendering stage are stored. Claim 33 recites a graphics system having a multi-stage processing pipeline configured to reissue geometric primitives for each sampling location of a sampling pattern, and for each time the geometric primitive is issued, shifting a transformed primitive by a sub-pixel offset corresponding to a respective one of the sampling locations of the sampling pattern and rendering the shifted primitive to generate values for pixels of a respective intermediate image.

The Zhu patent fails to at least describe a rendering stage that is configured to shift the geometric primitive a sub-pixel offset and calculate values for pixels representing the shifted geometric primitive. The Zhu patent further fails to disclose a multi-stage processing pipeline configured to reissue geometric primitives for each sampling location of a sampling pattern, and for each time the geometric primitive is issued. As previously discussed with respect to claims 1, 10, and 18, the Zhu patent is directed to a rendering pipeline utilizing SST and a double-z rendering scheme. Although cited by the Examiner for substantiating the anticipation rejection, the material cited by the Examiner fails to disclose the limitations for which they have been cited.

For the foregoing reasons, claims 24 and 33 are patentably distinct from the Zhu patent, and consequently, the rejection of claims 24 and 33 under 35 U.S.C. 102(e) must be withdrawn.

Dependent claims 2-9, 11, 13-17, 19-23, 25-32, and 34-36 are similarly patentably distinct from the Zhu patent based on their dependency from an allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. For the foregoing reasons, the rejection of claims 2-9, 11, 13-17, 19-23, 25-32, and 34-36 under 35 U.S.C. 102(e) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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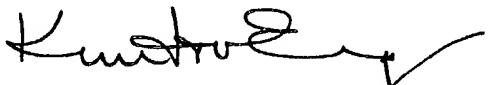

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